CLAIMS:

1. A receiver (RECEP) for receiving an input signal comprising a series of samples (IN_TIME, EARLY, LATE, VOID), said receiver (RECEP) comprising one delay line (D_LINE), characterized in that the delay line (D_LINE) is intended to delay said input signal by a series of delays (τ) and is divided into a series of delay sub-lines (ZONE) each intended to write one from the series of samples (IN_TIME, EARLY, LATE, VOID) of said input signal (INPUT), and in that the solution comprises control means (RD_ADD_GEN) intended to generate read addresses of the samples in the delay sub-lines (ZONE) from the series of samples (IN_TIME, EARLY, LATE, VOID) of the input signal (INPUT), so that a read address is equal to a difference between a write address of a sample in a delay sub-line (ZONE) of the input signal and a delay (τ) expressed as a number of sampling periods from the series of delays (τ).

2. A receiver (RECEP) as claimed in claim 1, characterized in that the delay line comprises a single series of delay sub-lines.

3. A receiver (RECEP) as claimed in claim 1, characterized in that the delay line comprises various series (BANK) of delay sub-lines.

4. A receiver (RECEP) as claimed in one of the preceding claims 1 to 3, characterized in that a delay sub-line (ZONE) is accessible with a frequency twice as fast as the samples of an input signal received by the receiver (RECEP).

5. A receiver (RECEP) as claimed in one of the preceding claims 1 to 4, characterized in that one memory area is associated to one delay sub-line (ZONE).

6. A receiver (RECEP) as claimed in one of the preceding claims 1 to 5, characterized in that the samples of a series of samples (IN_TIME, EARLY, LATE, VOID) are accessible in parallel in the write mode or read mode in the delay sub-lines (ZONE).

7. A receiver (RECEP) as claimed in one of the preceding claims 1 to 6, characterized in that the read addresses of the samples of a series of samples (IN_TIME, EARLY, LATE, VOID) are situated at addresses immediately adjacent or equal to one another.

8. A receiver (RECEP) as claimed in one of the preceding claims 3 to 7, characterized in that two series of samples (C_CHIP, NEXT_CHIP) are read in parallel.

9. A receiver (RECEP) as claimed in the preceding claim 8, characterized in that the delay line (D_LINE) comprises selection means (SELECT_BANK) of a series (BANK) of delay sub-lines to which belongs one of the two series of samples read as a function of the delay (τ).

10. A receiver (RECEP) as claimed in one of the preceding claims 1 to 9, characterized in that the delay line (D_LINE) comprises a position factor (DOWN_POS) indicating the position of a reference sample (IN_TIME) from a series of samples (IN_TIME, EARLY, LATE, VOID) of an input signal in the series of delay sub-lines to which it belongs.

11. A receiver (RECEP) as claimed in the preceding claim 8, characterized in that the memory areas (ZONE) are regrouped into a first and a second group (GROUPEA, GROUPEB), the first group regrouping a current series of current areas (C_BANK) and a next series of areas (NEXT_BANK) which can each correspond to the first series (BANK0) of delay sub-lines and the second group regrouping a current series of areas (C_BANK) and a next series of areas (NEXT_BANK) which can each correspond to the second series (BANK1) of the delay sub-lines, so that the memory areas for a series of samples read are identical for each equal position factor value (DOWN_POS).

12. A delay line (D_LINE) for delaying an input signal (INPUT), said input signal comprising a series of samples, (IN_TIME, EARLY, LATE, VOID), characterized in that the delay line is intended to delay said input signal by a series of delays (τ) and is divided into a series of delay sub-lines (ZONE) each intended to write one from the series of samples (IN_TIME, EARLY, LATE, VOID) of said input signal (INPUT), and in that the delay line comprises control means (RD_ADD_GEN) intended to generate read addresses of the samples in the delay sub-lines (ZONE) from the series of samples (IN_TIME, EARLY,

LATE, VOID) of the input signal (INPUT), so that a read address is equal to a difference between a write address of a sample in a delay sub-line (ZONE) of the input signal and a delay (τ) expressed as a number of sampling periods of the series of delays (τ).

13. A method of delaying an input signal (INPUT) by means of a delay line (D_LINE), said input signal comprising a series of samples (IN_TIME, EARLY, LATE), characterized in that it comprises the steps of:

- dividing the delay line (D_LINE) into a series of delay sub-lines (ZONE) each intended to receive a sample from the series of samples (IN_TIME, EARLY, LATE, VOID) of the input signal (INPUT), said delay line being intended to delay said input signal by a series of delays (τ), and
- generating read addresses of the samples in the delay sub-lines (ZONE) from the series of samples of the input signal (INPUT), so that a read address is equal to a difference between a write address of a sample in a delay sub-line (ZONE) of the input signal and a delay (τ) expressed as a number of sampling periods of the series of delays (τ).